a compiler for forming groups of instructions having opcodes including a first group of instructions and a second group of instructions, instructions in the first group of instructions executable in parallel, and instructions in the second group of instructions executable in parallel;

a first memory storage having at least a memory location, the memory location for storing the first group of instructions, for storing the second group of instructions comprising at least one instruction, and for storing group identifiers that indicate which instructions are included within the first group of instructions and which instructions are included within the second group of instructions;

a pre-decoder coupled to the first memory storage for decoding opcodes of instructions in the first group of instructions and opcodes of instructions in the second group of instructions, for forming a first group of expanded instructions, a second group of expanded instructions, and expanded group identifiers, and for determining processing pipeline identifiers associated with expanded instructions in the first group of expanded instructions and processing pipeline identifiers associated with expanded instructions in the second group of expanded instructions, in response thereto;

B1 cont.

a second memory storage coupled to the predecoder having at least a memory location, the memory location for storing the first group of expanded instructions, the second group of expanded instructions, the expanded group identifiers, the processing pipeline identifiers associated with the expanded instructions in the first group of expanded instructions, and the processing pipeline identifiers associated with the expanded instructions in the second group of expanded instructions;

a decoder coupled to the second memory storage for receiving the first group of expanded instructions, the second group of expanded instructions, and the expanded group identifiers, and for issuing the first group of expanded instructions in response to the expanded group identifiers;

a plurality of processing pipelines;

a crossbar coupled to the decoder and to the plurality of processing pipelines, for issuing expanded instructions in the first group of expanded instructions to processing

pipelines of the plurality of processing pipelines in response to the processing pipeline identifiers associated with the expanded instructions in the first group of expanded instructions.

26. (Amended) A method for issuing groups of individual software-scheduled instructions in parallel for processing comprises:

forming a first group of software-scheduled instructions, a second group of software-scheduled instructions comprising at least one instruction, and group identifiers indicating which software-scheduled instructions are included within the first group of software-scheduled instructions and which software-scheduled instructions are included within the second group of software-scheduled instructions, software-scheduled instructions in the first group of software-scheduled instructions having opcodes and executable in parallel, and software-scheduled instructions in the second group of software-scheduled instructions having opcodes and executable in parallel;

storing the first group of software-scheduled instructions, the second group of software-scheduled instructions, and the group identifiers in parallel in a first memory location;

forming a first group of expanded software-scheduled instructions, a second group of expanded software-scheduled instructions, and expanded group identifiers in response to opcodes of software-scheduled instructions in the first group of software-scheduled instructions and opcodes of software-scheduled instructions in the second group of software-scheduled instructions;

determining processing pipelines appropriate for expanded software-scheduled instructions in the first group of expanded software-scheduled instructions and processing pipelines appropriate for expanded software-scheduled instructions in the second group of expanded software-scheduled instructions also in response to the opcodes of software-scheduled instructions in the first group of software-scheduled instructions and the opcodes of software-scheduled instructions in the second group of software-scheduled instructions; and

issuing the first group of expanded software-scheduled instructions to the processing pipelines appropriate for expanded software-scheduled instructions in the first group of expanded software-scheduled ~~instructions~~, in response to the expanded group identifiers.

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49. (Amended) A method for issuing a group of individual instructions in parallel for processing comprises:

storing in parallel a plurality of instructions and instruction grouping information in a location in a memory, the plurality of instructions and the instruction grouping information determined by a compiler, the instruction grouping information indicating which instructions of the plurality of instructions belong to a first group of instructions and [are executable] can be issued in parallel, and indicating [which instructions] at least another instruction of the plurality of instructions [belong to a second group of instructions and are executable] that can be issued [in parallel] after the first group of instructions;

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issuing the first group of instructions in response to the instruction grouping information; and

coupling instructions in the first group of instructions to instruction pipelines appropriate for the instructions in the first group of instructions.

50. (Amended) The method of claim 49 further comprises

after [the step of] coupling instructions in the first group of instructions, issuing the [second group of instructions] the at least another instruction in response to the instruction grouping information; and

coupling [instructions in the second group of instructions] the at least another instruction to an instruction [pipelines] pipeline appropriate for the [instructions in the second group of instructions] at least another instruction .

51. (Amended) The method of claim 50 wherein the instruction grouping information also indicates which instructions of the plurality of instructions belong to a [third] second group of instructions and [are executable] can be issued in parallel after the [second group of instructions] the at least another instruction .

52. (Amended) The method of claim 49

wherein the instructions in the first group of instructions include instruction types; and

wherein [the step of] coupling instructions in the first group of instructions further comprises determining the instruction pipelines appropriate for the instructions in the first group of instructions in response to the instruction types.

53. (Amended) The method of claim 52 wherein the instruction types comprise opcodes.

54. (Amended) The method of claim [52] 50 wherein [the step of] issuing the first group of instructions further comprises receiving the first group of instructions, the [second group of instructions] at least another instruction , and the instruction grouping information from the location in the memory.

B3 Cont'

55. (Amended) The method of claim 50 wherein the [second] first group of instructions comprises at least two instructions.

56. (Amended) The method of claim [55] 50 wherein the first group of instructions comprises at least one instruction.

57. (Amended) The method of claim [56] 55 wherein an instruction frame comprises the plurality of instructions and instruction grouping information, and

B3 cancel

wherein the instruction frame includes at least the two instructions of the [second] first group of [software-scheduled] instructions and the at least [one] another instruction [of the first group of software-scheduled instructions] .

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61. (Amended) The method of claim 60 wherein [the step of] coupling instructions in the first group of instructions comprises using a crossbar switch to couple the instructions in the first group of instructions to the instruction pipelines appropriate for the instructions in the first group of instructions in response to the pipeline identifiers.

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63. (Amended) A computing system comprising:

a cache including a plurality of cache entries, a cache entry of the plurality of cache entries configured to store in parallel a plurality of software-scheduled instructions and instruction grouping information, the instruction grouping information configured to identify a first group of software-scheduled instructions from the plurality of software-scheduled instructions and to identify [a second group of] at least another software-scheduled [instructions] instruction from the plurality of software-scheduled instructions, [instructions in the second group of] the at least another software-scheduled [instructions] instruction to be issued after instructions in the first group of software-scheduled instructions [, each instruction in the first group of software-scheduled instructions including an instruction type] .

64. (Amended) The computing system of claim 63 wherein the instruction grouping information is also configured to identify a [third] second group of software-scheduled instructions from the plurality of software-scheduled instructions, instructions in the [third] second group of software-scheduled instructions to be issued after [instructions in the second group of] at least another software-scheduled [instructions] instruction .

65. (Amended) The computing system of claim 63

wherein the cache is also configured to issue the first group of software-scheduled instructions, the [second group of] at least another software-scheduled [instructions] instruction , and the instruction grouping information;

the computing system further comprising a group decoder coupled to the cache and configured to receive the first group of software-scheduled instructions, the [second group of] at least another software-scheduled [instructions] instruction , and the instruction grouping information, and to issue the first group of software-scheduled instructions in response to the instruction grouping information.

66. (Amended) The computing system of claim 65 wherein the group decoder is also configured to issue the [second group of] at least another software-scheduled [instructions] instruction , after the first group of software-scheduled instructions in response to the instruction grouping information.

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67. (Amended) The computing system of claim 65

wherein each instruction in the first group of software-scheduled instructions includes an instruction type,

the computing system further comprising [:] an instruction decoder coupled to the cache and configured to receive the instruction types of the instructions in the first group of software-scheduled instructions and to determine instruction pipelines appropriate for each of the instructions in the first group of software-scheduled instructions.

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73. (Amended) The computing system of claim 72 wherein an instruction frame comprises the plurality of software-scheduled instructions and instruction grouping information; and wherein the instruction frame includes at least the two instructions of the first group of software-schedule instructions and the [one instruction of the second group of] at least another software-scheduled [instructions] instruction .

B6 cont.

74. (Amended) The computing system of claim [76] 63 wherein the cache is a superscaler cache.

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76. (Amended) The computing system of claim [65] 67 wherein the instruction types comprise pipeline identifiers indicative of instruction pipelines appropriate for the instructions in the first group of software-scheduled instructions.

--77. (New) The method of claim 49 wherein the instruction grouping information also indicates instruction pipelines appropriate for the instructions in the first group of instructions; and

wherein coupling instructions in the first group of instructions to the instruction pipelines appropriate for the instructions in the first group of instructions is in response to the instruction grouping information.

B8

78. (New) The method of claim 77 wherein the instruction grouping information also indicates instruction pipelines appropriate for the instructions in the second group of instructions.

79. (New) The computing system of claim 65 further comprising an switching unit coupled to the cache and configured to receive the instructions in the first group of software-scheduled instructions and to couple the instructions in the first group of software-scheduled instructions to instruction pipelines appropriate for each of the instructions in the first group of software-scheduled instructions in response to the instruction grouping information.

80. (New) The computing system of claim 79 wherein the switching unit is also configured to receive the at least another software-scheduled instruction and to couple the at least another software-scheduled instruction to an instruction pipeline appropriate the at

least another software-scheduled instruction in response to the instruction grouping information.

81. (New) A computing system in which instructions are issued in parallel to processing pipelines, the computing system comprising:

a storage configured to store an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the instruction frame also including data associated with the plurality of instructions, the data associated with the plurality of instructions indicative of which instructions in the plurality of instructions are included in the group of instructions, the data associated with the plurality of instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at a compile time; and

a switching circuit coupled to the storage, configured to issue the instructions in the group of instructions in parallel, to processing pipelines appropriate for the instructions in the group of instructions, in response to the data associated with the plurality of instructions.

82. (New) The computing system of claim 81 wherein the group of instructions comprises at least two instructions.

83. (New) The computing system of claim 81 wherein the group of instructions comprises one instruction.

84. (New) The computing system of claim 81 wherein the switching circuit is also configured to issue the at least another instruction to a processing pipeline appropriate for the at least another instruction in response to the data associated with the plurality of instructions.

85. (New) The computing system of claim 81 wherein the processing pipelines appropriate for the instructions in the group of instructions are respectively coupled to execution units appropriate for the instructions in the group of instructions.

86. (New) The computing system of claim 85 wherein an execution unit appropriate for a first instruction in the group of instructions is a memory.

87. (New) The computing system of claim 86 wherein an execution unit appropriate for a second instruction in the group of instructions is an arithmetic logic unit.

88. (New) The computing system of claim 86 wherein an execution unit appropriate for a second instruction in the group of instructions is a floating point unit.

89. (New) The computing system of claim 85 wherein an execution unit appropriate for one instruction in the group of instructions is a branch unit.

90. (New) The computing system of claim 85 wherein a type of execution unit appropriate for a first instruction in the group of instructions and a type of execution unit appropriate for a second instruction in the one group of instructions are similar.

91. (New) The computing system of claim 81 wherein the plurality of instructions in the instruction frame are determined at the compile time.

92. (New) A method for issuing groups of instructions in parallel to processing pipelines, the method comprising:

storing in a storage, an instruction frame, the instruction frame including a plurality of instructions including a group of instructions and at least another instruction in parallel, instructions in the group of instructions to be issued in parallel, the instruction frame also including data fields associated with the plurality of instructions, the data associated with the plurality of instructions indicative of which instructions are included in the group of

instructions, the data associated with the instructions also indicative of processing pipelines appropriate for the plurality of instructions, and the data associated with the plurality of instructions determined at compile time; and

issuing the instructions in the group of instructions in parallel to processing pipelines appropriate for the instructions in the group of instructions, in response to the data associated with the plurality of instructions.

93. (New) The method of claim 92 further comprising:

during compile time, determining the plurality of instructions in the instruction frame.

94. (New) The method of claim 92 wherein the group of instructions comprises at least two instructions.

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95. (New) The method of claim 94 further comprising, before issuing the group of instructions, issuing the at least another instruction to a processing pipeline appropriate for the at least another instruction in response to the data associated with the plurality of instructions.

96. (New) The method of claim 92 wherein the processing pipelines appropriate for the instructions in the group of instructions are respectively coupled to execution units appropriate for the instructions in the group of instructions.

97. (New) The method of claim 96 wherein a type of execution unit appropriate for a processing pipeline appropriate for a first instruction in the group of instructions is an arithmetic logic unit.

98. (New) The method of claim 97 wherein a type of execution unit appropriate for a processing pipeline appropriate for a second instruction in the group of instructions is an arithmetic logic unit.

99. (New) The method of claim 96 wherein a type of execution unit appropriate for a processing pipeline appropriate for a first instruction in the group of instructions is a floating point unit.

100. (New) The method of claim 96 wherein a type of execution unit appropriate for a processing pipeline appropriate for a first instruction in the group of instructions is a memory unit and a type of execution unit appropriate for a processing pipeline appropriate for a second instruction in the group of instructions is a memory unit.

101. (New) A method of operating a microprocessor comprises:

compiling computer code to determine a frame of instructions;

storing in a memory storage the frame of instructions, the frame of instructions including a plurality of instructions and issue data, the plurality of instructions including at least a first instruction, a second instruction, and a third instruction, the issue data comprising data indicating that the first instruction is to be issued before the second instruction and the third instruction and the second and third instructions are to be issued in parallel, and the issue data indicating respective processing units appropriate for the first instruction, the second instruction, and the third instruction; and

issuing the first instruction to a processing unit appropriate for the first instruction in response to the issue data; and

issuing the second instruction and the third instruction in parallel to respective processing units appropriate for the second instruction and the third instruction in response to the issue data.

102. (New) The method of claim 101 wherein the processing unit appropriate for the first instruction is a memory unit.